The opinion in support of the decision being entered today was
<u>not</u> written for publication and is <u>not</u> binding precedent of the
Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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<u>Ex parte</u> RONALD X-ARROYO, WILLIAM E. BURKY and JODY BERN JOYNER

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Appeal No. 2001-2638
Application 09/201,214

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ON BRIEF

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Before KRASS, JERRY SMITH and FLEMING, <u>Administrative Patent
Judges</u>.

JERRY SMITH, <u>Administrative Patent Judge</u>.

<u>DECISION ON APPEAL</u>

        This is a decision on the appeal under 35 U.S.C. § 134

from the examiner's final rejection of claims 1-9 and 21-30,

which constituted all the claims in the application. First and

second amendments after final rejection were filed on January 15,

2001 and February 7, 2001 respectively. Neither of these

amendments was entered by the examiner. A third amendment after

final rejection was filed on February 22, 2001 and was entered by

the examiner. This amendment cancelled claims 2-9 and 22-26.

Therefore, this appeal is directed to the rejection of claims 1,

21 and 27-30.

The disclosed invention pertains to a memory controller

for managing memory operations in a data processing system. One

particular aspect of the invention is the manner in which memory

requests from an input/output device to a data processor are

handled.

Representative claim 1 is reproduced as follows:

1. A method for managing memory operations in a data
processing system using a memory controller having a device bus
interface, a memory interface and a system bus interface, said
method comprising the steps of:

receiving a memory request from a device bus interface
at a memory controller having a store buffer;

responsive to receiving said memory request, satisfying
said memory request asynchronously with said memory request via a
transaction on one of said system bus interface or said memory
interface, utilizing said store buffer to schedule said
transaction by transferring a processor's cache data to a device
coupled to said device bus by reading said processor's cache data
posted in one or more arrays within said memory controller.

The examiner relies on the following references:

Abramson et al. (Abramson)	5,751,983	May 12, 1998
Panwar et al. (Panwar)	6,058,472	May 02, 2000
		(filed June 25, 1997)
Kaiser et al. (Kaiser)	EP 0 766 179	Apr. 02, 1997

Claims 1, 21 and 27-30 stand rejected under 35 U.S.C. § 103(a). As evidence of obviousness the examiner offers Kaiser in view of Panwar or Abramson.

Rather than repeat the arguments of appellant or the examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in the claims on appeal. Accordingly, we reverse.

Appellants have indicated that for purposes of this appeal the claims will all stand or fall together as a single group [brief, page 6]. Consistent with this indication appellants have made no separate arguments with respect to any of the claims on appeal. Accordingly, all the claims before us will stand or fall together. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983). Therefore, we will consider the rejection against independent claim 1 as representative of all the claims on appeal.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in

the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044,

1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S.

825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories,

Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985),

cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v.

Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed.

Cir. 1984). These showings by the examiner are an essential part

of complying with the burden of presenting a prima facie case of

obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d

1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden

then shifts to the applicant to overcome the prima facie case

with argument and/or evidence. Obviousness is then determined on

the basis of the evidence as a whole and the relative

persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d

1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki,

745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and

In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA

1976). Only those arguments actually made by appellants have

been considered in this decision. Arguments which appellants

could have made but chose not to make in the brief have not been

considered and are deemed to be waived [see 37 CFR § 1.192(a)].

With respect to representative claim 1, the examiner
cites Kaiser as teaching the claimed invention except that there
is no description in Kaiser of the store buffer which the
examiner has read on the "system read/write Q" and the "memory
read/write Q" of Kaiser. The examiner cites Panwar as teaching a
memory controller including a disambiguation buffer (MDB) that
has a store buffer. The examiner cites Abramson as teaching a
memory controller which has a store buffer. The examiner finds
that it would have been obvious to the artisan to replace the
system read/write Q and the memory read/write Q of Kaiser with
the MDB of Panwar which would allegedly result in the claimed
invention. The examiner also finds that it would have been
obvious to the artisan to operate the read/write Qs of Kaiser in
the same manner as Abramson operates the reservation stations
which would also allegedly result in the claimed invention
[answer, pages 4-6].

Appellants argue that the system read/write Q and the
memory read/write Q of Kaiser do not show or suggest a buffer
which may be utilized to schedule a memory request transaction in
the manner recited in independent claims 1 and 21. Appellants
also argue that neither Panwar nor Abramson teaches or suggests
the transfer of a processor's cache that has been stored in a

memory controller to a device as set forth in the claimed

invention [brief, pages 6-9].

        The examiner responds that the course of prosecution in

this application led to the obviousness issue hinging on the

"topology" of appellants' invention. The examiner notes that

Kaiser was cited only to show this topology and that the

deficiencies of the read/write Qs of Kaiser are not relevant.

The examiner also responds that in a system where a single

controller connects all of the busses as in Kaiser, it clearly

follows that it would have been obvious to service load requests

from the device bus out of the store buffer since the memory

controller is directly connected to the device bus [answer, pages

7-8].

        We will not sustain the examiner's rejection. Although

the examiner suggests that we should draw certain inferences on

the question of obviousness based on the course of prosecution in

this case, we decline to do so. We must consider the claimed

invention and the clear teachings of the applied prior art.

Representative claim 1 recites that data which originated in a

processor's cache is transferred to a device bus using the store

buffer of the memory controller. As noted by appellants, the

store buffer of Kaiser (the system and memory read/write Qs) is

not described within the patent. Despite the fact that there is
absolutely no discussion of how the read/write Qs of Kaiser
operate, the examiner selects memory controllers from Panwar or
Abramson to replace the read/write Qs of Kaiser. There is
nothing within the applied prior art to suggest that the
controllers of Panwar or Abramson could or should replace the
controller of Kaiser. In addition, the memory controllers of
Panwar and Abramson are used to control memory read/write
requests between a data processor and a memory. There is no
suggestion within Panwar or Abramson that their memory
controllers should be used in the manner recited in claim 1 for
communication of data between the data processor and external
devices. The examiner's assertion that it would clearly have
been obvious to use the store buffer of a memory controller in
this type of communication is based on nothing except the
examiner's bare opinion and a need to reconstruct the claimed
invention. While there may be evidence to support the
obviousness of the claimed invention, the examiner has not
provided the evidence which is needed to support the examiner's
rejection.

In summary, we have not sustained the examiner's

rejection of the claims on appeal. Therefore, the decision of

the examiner rejecting claims 1, 21 and 27-30 is reversed.

<u>REVERSED</u>

ERROL A. KRASS   )
Administrative Patent Judge   )
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)
) BOARD OF PATENT
JERRY SMITH   )
Administrative Patent Judge   )   APPEALS AND
)
) INTERFERENCES
)
MICHAEL R. FLEMING   )
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JS/dym

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